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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,243	07/09/2003	Mitsunori Matsunaga	402695	8347

23548 7590 10/13/2004

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EXAMINER	
CHAN, EMILY Y	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 10/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,243	MATSUNAGA ET AL.	
	Examiner	Art Unit	
	Emily Y Chan	2829	AU

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4 and 5* is/are allowed.

6)☒ Claim(s) *1-3 and 6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7-9-03*, 10/01
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-3 and 6 are rejected under 35 U.S.C. 102 (b) as being anticipated by Makoto Ishizawa ('106).

Regarding to claims 1 and 6, Makoto Ishizawa ('106) discloses a burn-in test adapter (trial board 9) as claimed, comprising an assembly substrate (socket 10), a plurality of semiconductor chip (3), each having terminal for receiving a burn-in test waveform (2), a wiring (conductive interconnects) for, when the assembly substrate (10) is attached to burn-in test adapter (trial board 9), making electrical contact with terminals of each of the semiconductor chips (3) on the assembly substrate (10) (see paragraph 0017, lines 4-5), and a burn-in test terminal (contact pin) electrically connected to the wiring and receiving the burn-in test waveform (2) (see paragraph 0018).

2. Regarding to claim 2, Makoto Ishizawa ('106) discloses a burn-in test waveform generation circuit (see Fig. 2 waveform pattern generator 22).

3. Regarding to claim 3, Makoto Ishizawa ('106) discloses that his burn-in test adapter (trial board 9) is square shape which encompasses the scope of the claimed burn-in test adapter that is rectangular. Makoto Ishizawa ('106) also discloses that his

burn-in test terminal (contact pin) is located on one of the four sides of the burn-in test adapter (trial board 9) (see fig 2).

4. Regarding to claim 6, Makoto Ishizawa ('106) discloses a burn-in test adapter (20) having an assembly substrate (10) on which a plurality of semiconductor chips (12) each having a chip-side for receiving a burn-in waveform (2) are arranged (paragraph 0017 lines 3-5), comprising: an adapter-side terminal (a contact pin) corresponding to each chip–side terminal (see Fig. 2 and paragraph (0018), lines 1-3), a signal receiving terminal (7, 8) for receiving the burn-in test waveform and a wiring (conductive interconnects) for electrically connecting the adapter-side terminal (contact pin) to the signal receiving terminal (7, 8).

Therefore, Makoto Ishizawa ('106) anticipates the claimed invention.

Allowable Subject Matter

5 Claims 4-5 are allowed.

The following is an examiner's statement of reasons for allowance:

Claims 4-5 are indicated allowable because the prior art does not teach or suggest a burn-in test apparatus with detail of all the elements recited in claim 4. Specifically, the prior art does not teach the combination that the burn-in apparatus comprising a burn-in test adapter having a assembly substrate, a first wiring for, when the assembly substrate is attached to the burn-in test adapter, making an electrical contact with terminals of each of the semiconductor chips on the assembly substrate, a bun-in test terminal that is electrically connected to the first wiring and receives a burn-in test waveform and is located on one of the four sides of the burn-in test adapter, a

socket that holds the burn-in test adapter at the side on which the burn-in test terminal is located and that is electrically connected to the bum-in test terminal, and a burn-in board that holds the socket and that includes a second wiring that is electrically connected to the socket and receives the burn-in test waveform. Claim 5 depends on claim 4 and indicated allowable accordingly.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Malhi et al ('792) disclose a burn-in test apparatus comprising a socket adapter (20) an assembly substrate (24) is attached to the burn-in test adapter (20), wiring (34) for when the assembly substrate (24) is attached to the burn-in adapter (20), making an electrical contact with the terminals of each of the semiconductor chips (12) on the assembly substrate (24).

Fehrman ('981) disclose a universal power interface adapter for burn-in board comprising a test socket (74) and burn-in board (12) (see Fig. 6).

Hembree et al ('323) disclose testing apparatus such as a burn-in board wherein a temporary package for testing semiconductor dice can be mounted (see Figs 2-5).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emily Y Chan whose telephone number is 571-272-1956. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ec
9-21-04

DAVID ZARNEKE
PRIMARY EXAMINER
9/15/04